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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,693	06/26/2003	Hiroki Sato	SON-2780	2889

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EXAMINER	
MADDEN, GREGORY VINCENT	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,693	SATO ET AL.	
	Examiner	Art Unit	
	Gregory V. Madden	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

First, in regard to claims 1 and 10, Applicant has amended the claims to include "...that the driving circuit performs a high-speed reading operation for selecting pixels at a higher speed than under normal reading operations, and that the high-speed reading operation is used to output a pixel output signal to a pixel defect determining circuit" (See Remarks/Arguments, Pg. 7). Applicant argues that the Takayama reference (U.S. Pat. 6,683,643) fails to teach the concept of using a high-speed reading operation for a pixel defect testing method, as the amended claims state. While the Examiner agrees that Takayama alone does not teach the above limitation, the Applicant's arguments are considered moot in view of the new ground of rejection citing Shimura (U.S. Pat. 6,307,393). As will be set forth below, the Shimura reference teaches the concept of using a high-speed reading operation for a pixel defect testing method, and thus reads on the Applicant's newly amended claims 1 and 10.

As for claims 4, 5, and 11, it is noted that Applicant has canceled claim 4, and the Applicant further argues that the Oda reference (U.S. Pat. 6,340,989) fails to teach the high-speed reading operation to be used during pixel defect testing, as claimed by the Applicant. Specifically, the Applicant argues that "...Oda achieves its 'high speed' reading operation by omitting entire lines of pixels in its reading scheme. Such reading operations are completely unsuitable for use in pixel testing where all of the pixels must be read to determine if they are defective" (See Remarks/Arguments, Pg. 10). Again the Examiner agrees that the combination of Takayama in view of Oda does not sufficiently teach the limitations of claims 5 and 11, but the Applicant's arguments are considered moot in view of the new ground of

rejection citing Shimura (U.S. Pat. 6,307,393). Please refer to the new rejection of claims 5 and 11 below.

Next, in regard to claims 6-9, 12, and 13, the Applicant again argues that the Takayama reference fails to teach the limitations of claims 1 and 10, and thus the limitations of claims 6-9, 12, and 13 are not met by the combination of Takayama in view of Oda further in view of Kidono et al. (U.S. Pat. 6,970,193). Again, the Examiner agrees that Takayama alone fails to teach the limitations of newly amended claims 1 and 10, but the Applicant's arguments are considered moot in view of the new ground of rejection citing Shimura (U.S. Pat. 6,307,393). Please refer to the updated rejection to claims 6-9, 12, and 13 below.

Considering claim 14, the Applicant argues that the limitation of a predetermined test signal being input to other circuits on the chip in parallel with a defect test on the pixel unit is not common and well known in the art, and therefore the Official Notice taken by the Examiner in regard to the limitations of claim 14 is improper. The Examiner agrees with the Applicant, and thus the previous rejection of claim 14 is whereby withdrawn.

Finally, the Examiner notes that the Applicant has amended the drawings to include a "Prior Art" label on Fig. 11. With this amendment, the drawings are considered to be acceptable, and therefore the previous objection to the drawings is hereby withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 5-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimura (U.S. Pat. 6,307,393).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

First, considering **claim 1**, the Shimura reference teaches a solid-state image pickup device comprising a pixel unit (CCD 3) including a plurality of unit pixels that perform photoelectric conversion, a driving circuit (driver 7) for driving the pixel unit to control output of a pixel output signal, the driving circuit (7) having a function of performing a normal reading operation (i.e. normal image sensing mode) for selecting pixels at a normal speed (storage time set for a period of six fields), and a high-speed reading operation (defect detection mode) for selecting pixels at a higher speed than that under the normal reading operation (i.e. storage time set for a period of only four fields). Further, Shimura teaches that the device comprises an output signal processing circuit (signal processing circuit 12) for subjecting the pixel output signal outputted from the pixel unit (3) during the normal reading operation performed by the driving circuit (7) to predetermined signal processing and outputting a resulting pixel output signal (to encoder 13), a pixel defect determining circuit (defect detection circuit 10) for capturing the pixel output signal outputted from the pixel unit (3) during the high-speed reading operation (i.e. in the defect detection mode) performed by the driving circuit (7), and determining a pixel defect by comparing the pixel output signal with a predetermined reference signal (detection reference level), and finally a timing generator

(timing generator 6) for supplying a predetermined operating pulse to the driving circuit (7), the output signal processing circuit, and the pixel defect determining circuit. Please refer to Figs. 1 and 3, and Col. 4, Line 54 – Col. 5, Line 34, and Col. 6, Lines 54 – Col. 8, Line 46.

As for **claim 2**, the limitations of claim 1 are taught above, and Shimura further discloses that the device comprises a selecting circuit (microcomputer 4) for selectively operating the output signal processing circuit (12) in a normal output mode and the pixel defect determining circuit (10) in a defect test mode (i.e. defect detection mode), as is shown in Col. 5, Lines 1-15, and Col. 6, Lines 53 – Col. 7, Line 62.

In regard to **claim 3**, again the limitations of claim 1 are taught above, and the Shimura reference teaches that the driving circuit reads out the pixels of the pixel unit by a pixel row (e.g. by fields), as is shown in Col. 5, Lines 16-24.

Next, considering **claim 5**, the limitations of claim 1 are set forth above, and Shimura discloses that the driving circuit (7) selects a pixel to read out a signal under the high-speed reading operation (during defect detection mode) in a time of testing the pixel unit for a defect. See Col. 6, Lines 53 – Col. 7, Line 62.

Considering **claim 6**, the limitations of claim 1 are again taught above, and Shimura also teaches that the normal reading operation comprises selecting pixels to read out a signal by a pixel row (in a six field readout), while the high-speed reading operation (defect detection mode) comprises selecting more pixels to read out a signal (i.e. a four field readout) than that under the normal reading operation. Please refer once again to Col. 6, Lines 53 – Col. 7, Line 62.

As for **claim 7**, the limitations of claim 6 are taught above, and as is similarly shown with respect to claim 5 above, Shimura discloses that the driving circuit (7) selects a pixel to read out a signal under the high-speed reading operation (during defect detection mode) in a time of testing the pixel unit for a defect. See Col. 6, Lines 53 – Col. 7, Line 62.

Regarding **claim 8**, the limitations of claim 1 are again taught above, and Shimura also teaches that the normal reading operation comprises selecting pixels to read out a signal by a pixel row (in a six field readout), while the high-speed reading operation (defect detection mode) comprises selecting more pixels to read out a signal (i.e. a four field readout) than that under the normal reading operation at a higher speed than under the normal reading operation (i.e. four field readout occurs at a higher speed than six field readout). Please refer once again to Col. 6, Lines 53 – Col. 7, Line 62.

Considering **claim 9**, the limitations of claim 8 are shown above, and Shimura discloses that the driving circuit (7) selects a pixel to read out a signal under the high-speed reading operation (during defect detection mode) in a time of testing the pixel unit for a defect. See Col. 6, Lines 53 – Col. 7, Line 62.

Next, in regard to **claim 10**, the Shimura reference teaches a pixel defect testing method for a solid-state image pickup device, wherein the solid-state image pickup device comprises a pixel unit (CCD 3) including a plurality of unit pixels that perform photoelectric conversion, a driving circuit (driver 7) for driving the pixel unit to control output of a pixel output signal, an output signal processing circuit (signal processing circuit 12) for subjecting the pixel output signal outputted from the pixel unit (3) according to the driving of the driving circuit (7) to predetermined signal processing and outputting a resulting pixel output signal (to encoder 13), and a timing generator (timing generator 6) for supplying a predetermined operating pulse to the driving circuit (7) and the output signal processing circuit. Further, Shimura teaches that the driving circuit (7) functions to perform a normal reading operation for selecting pixels at a normal speed (normal image sensing mode) and a high-speed operation for selecting pixels at a higher speed than under the normal reading operation (defect detection mode), wherein the pixel output signal output from the pixel unit during the high-speed operation performed by the driving circuit is captured independently of the output signal processing circuit (note that defect detection circuit 10 is independent of signal processing circuit 12), and a pixel defect is determined by comparing the captured pixel output

signal with a predetermined reference signal (detection reference level), and a defect test on the captured pixel output signal outputted from the pixel unit is performed on the basis of an operating pulse from the timing generator (6). Please refer to Figs. 1 and 3, and Col. 4, Line 54 – Col. 5, Line 34, and Col. 6, Lines 54 – Col. 8, Line 46.

As for **claim 11**, the limitations of claim 10 are taught above, and Shimura further teaches that the driving circuit (7) selects a pixel to read out a signal under the high-speed reading operation (during defect detection mode) in a time of testing the pixel unit for a defect. See Col. 6, Lines 53 – Col. 7, Line 62.

Regarding **claim 12**, again the limitations of claim 10 are set forth above, and Shimura discloses that the driving circuit (7) selects more pixels (i.e. a four field readout) during the high-speed reading operation (defect detection mode) than at the time of the normal reading operation (normal image sensing mode) in a time of testing the pixel unit for a defect. Please refer once again to Col. 6, Lines 53 – Col. 7, Line 62.

Finally, considering **claim 13**, the limitations of claim 10 are taught above, and Shimura also teaches that the driving circuit, while the high-speed reading operation (defect detection mode), selects more pixels to read out a signal (i.e. a four field readout) than that under the normal reading operation at a higher speed than under the normal reading operation (i.e. four field readout occurs at a higher speed than six field readout). Please refer once again to Col. 6, Lines 53 – Col. 7, Line 62.

Allowable Subject Matter

Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regard to **claim 14**, the prior art was not found to teach or reasonably suggest, in combination with all of the limitations of claim 10, a pixel defect testing method wherein in parallel with a defect test on a pixel unit, a predetermined test signal is inputted to other circuits on the same chip and a defect test on the other circuits on the same chip is performed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kameyama et al. (U.S. Pat. 5,416,516)

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory V. Madden whose telephone number is 571-272-8128. The examiner can normally be reached on Mon.-Fri. 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc Yen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gregory Madden
March 22, 2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER